

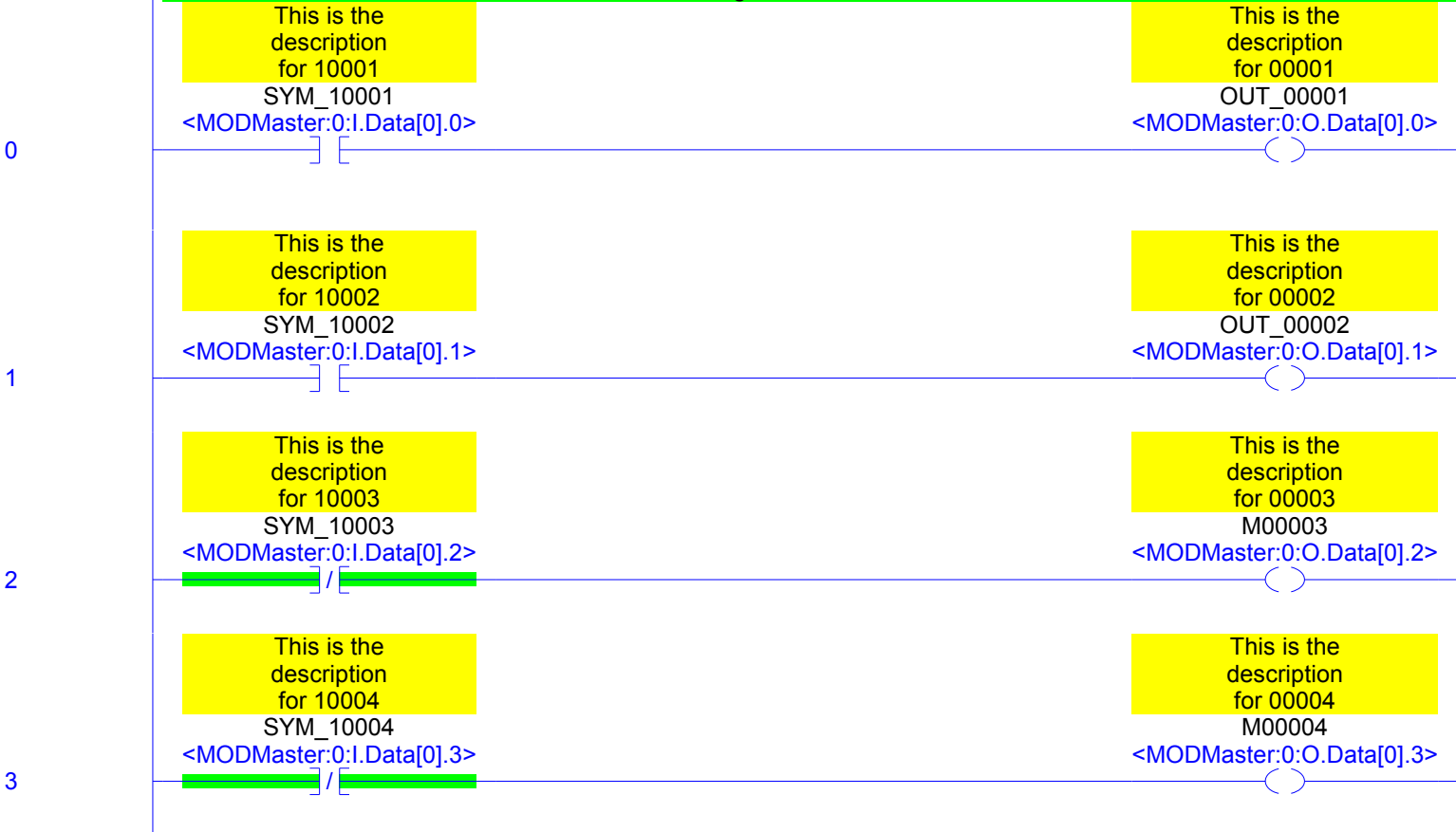


Network 1
This is the page title - Bits
This is the short comment for N0001
This program is totally useless...

as far as controlling any process. Now on the other hand if you would like to see how different instructions are converted read on.

This program was converted using the ANX option. The registers convert to alias' that point to the AN-X module. The AN-X CSV file has been imported into the ControlLogix program.

This section of rungs show how bits are converted.



4

This is the description for 10005
SYM_10005
<MODMaster:0:I.Data[0].4>

This is the description for 10006
M10006
<MODMaster:0:I.Data[0].5>

This is the description for 10007
M10007
<MODMaster:0:I.Data[0].6>

This is the description for 10008
M10008
<MODMaster:0:I.Data[0].7>

This is the description for 10009
M10009
<MODMaster:0:I.Data[0].8>

This is the description for 10010
M10010
<MODMaster:0:I.Data[0].9>

This is the description for 10011
M10011
<MODMaster:0:I.Data[0].10>

This is the description for 10012
M10012
<MODMaster:0:I.Data[0].11>

This is the description for 10013
M10013
<MODMaster:0:I.Data[0].12>

This is the description for 10014
M10014
<MODMaster:0:I.Data[0].13>

This is the description for 10015
M10015
<MODMaster:0:I.Data[0].14>

This is the description for 10016
M10016
<MODMaster:0:I.Data[0].15>

This is the description for 00005
M00005
<MODMaster:0:O.Data[0].4>

Network 2

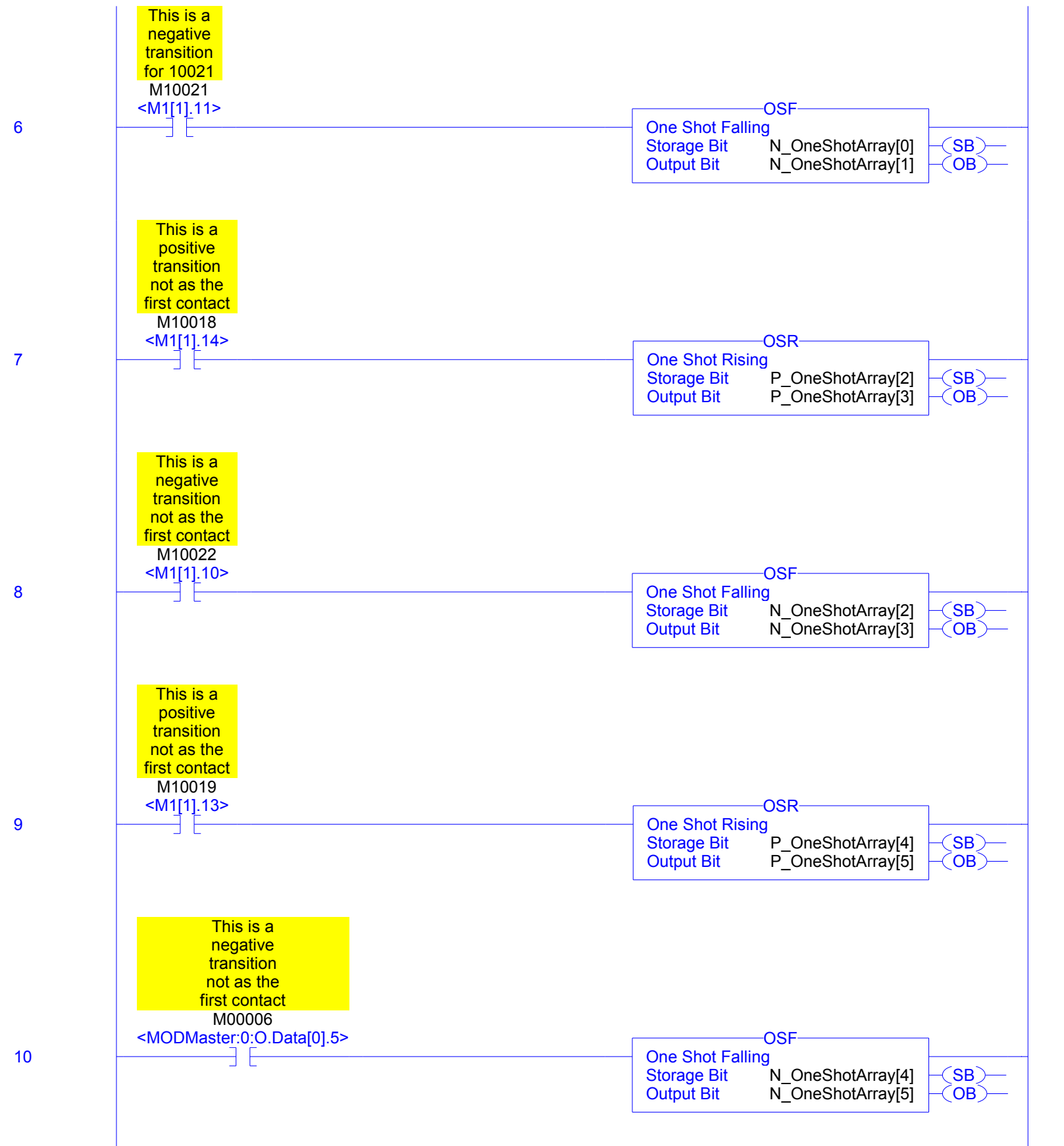
5

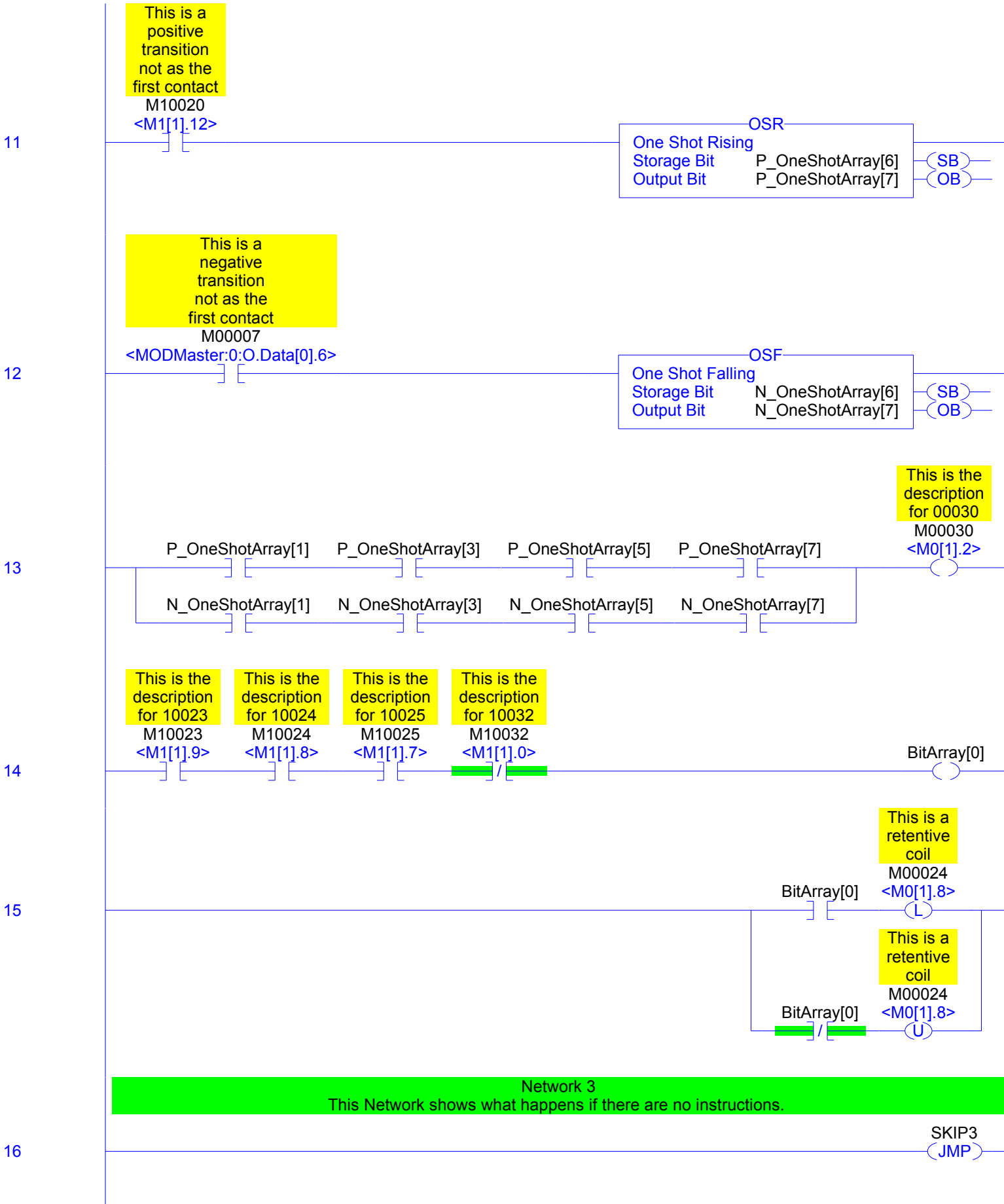
This is a positive transition for 10017
M10017
<M1[1].15>

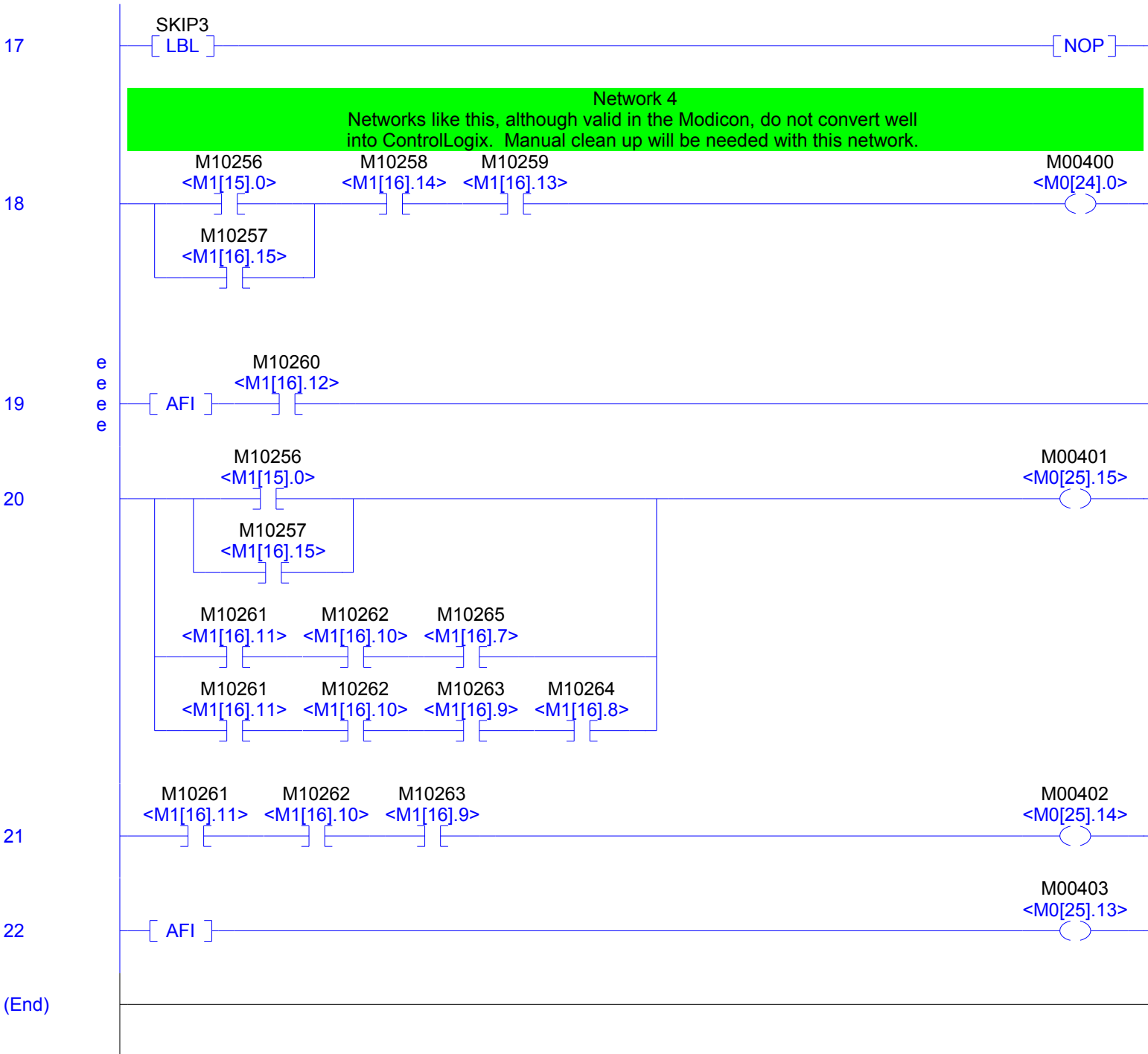
OSR

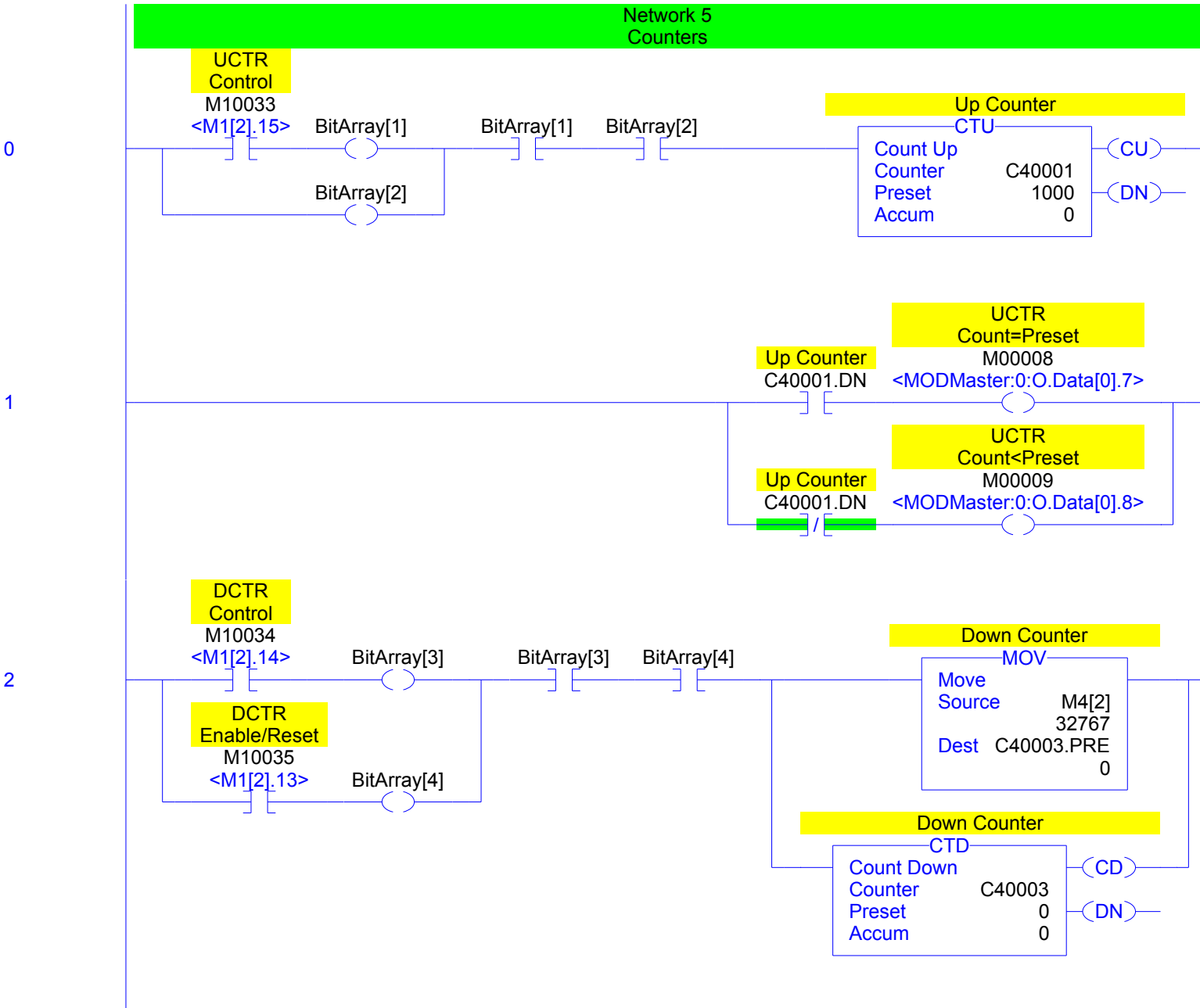
One Shot Rising Storage Bit P_OneShotArray[0] (SB)

Output Bit P_OneShotArray[1] (OB)









3

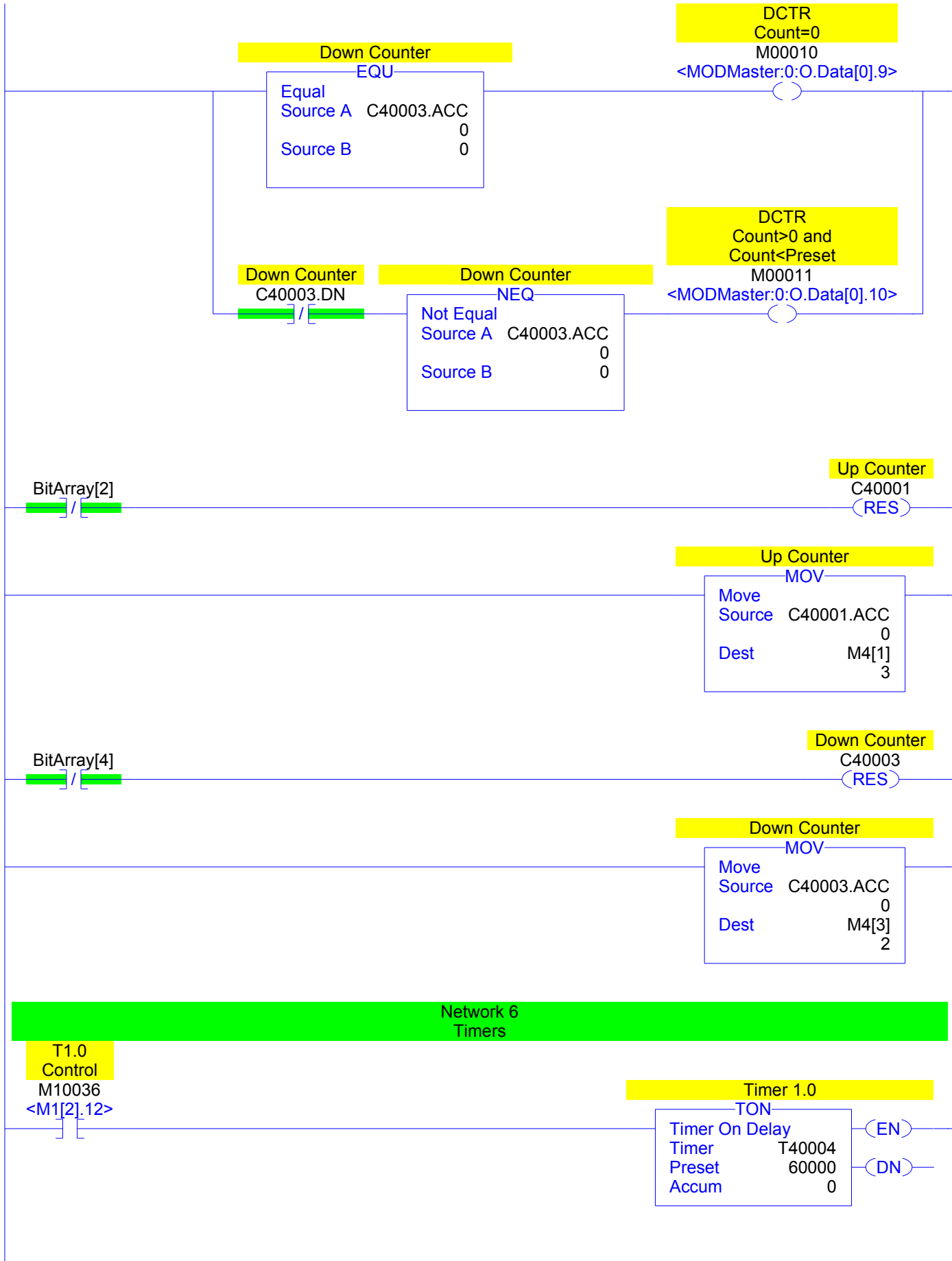
4

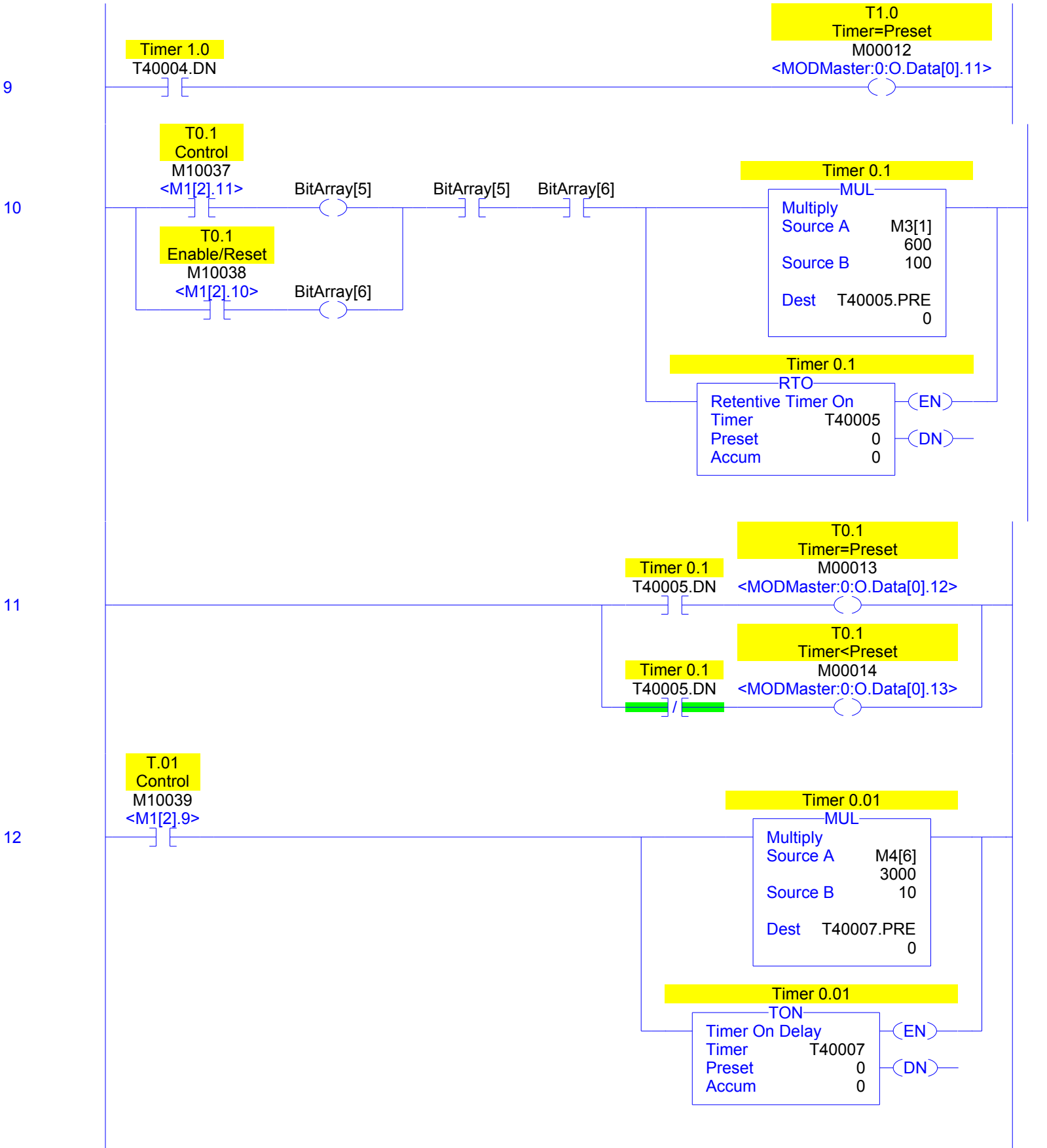
5

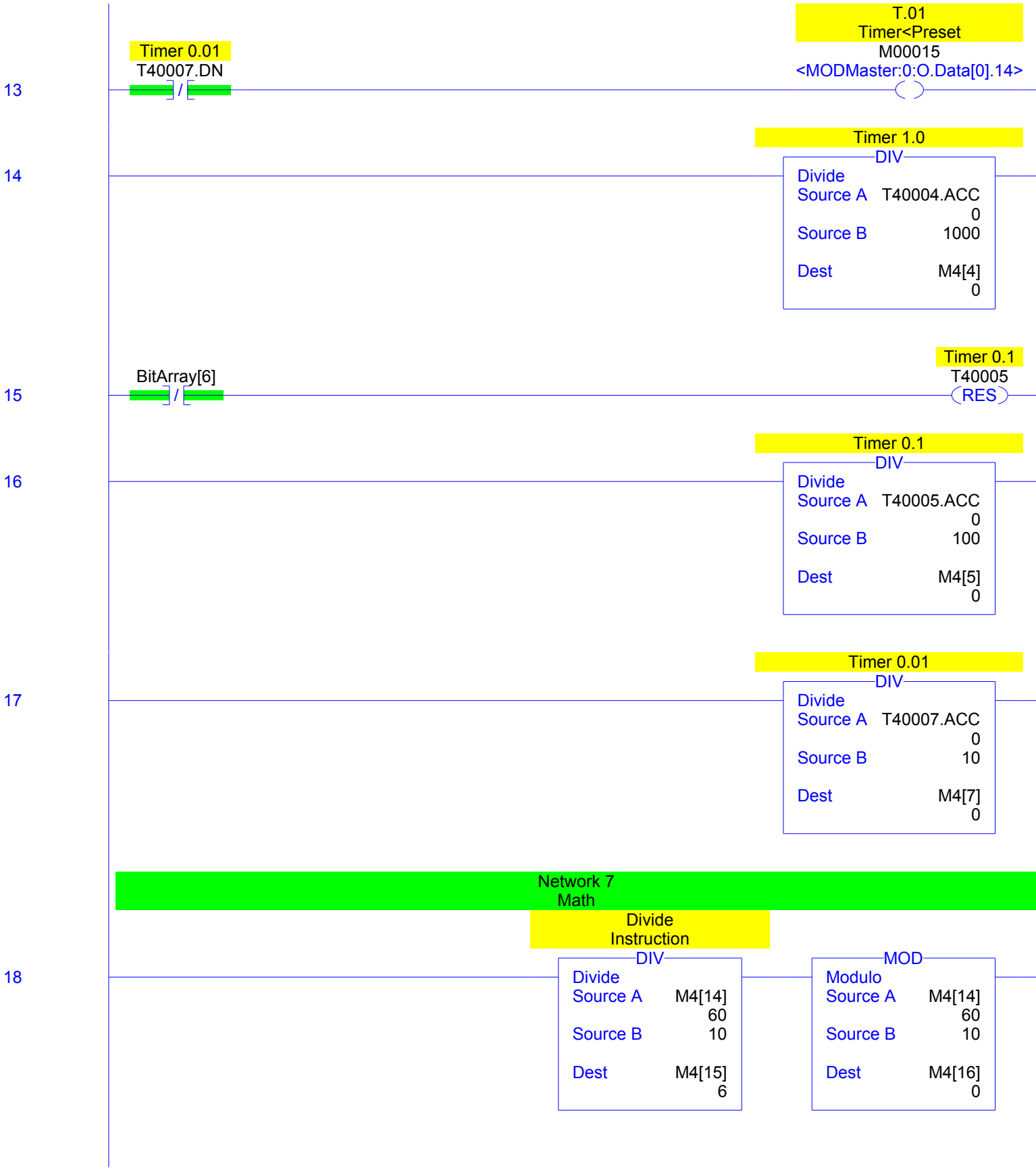
6

7

8

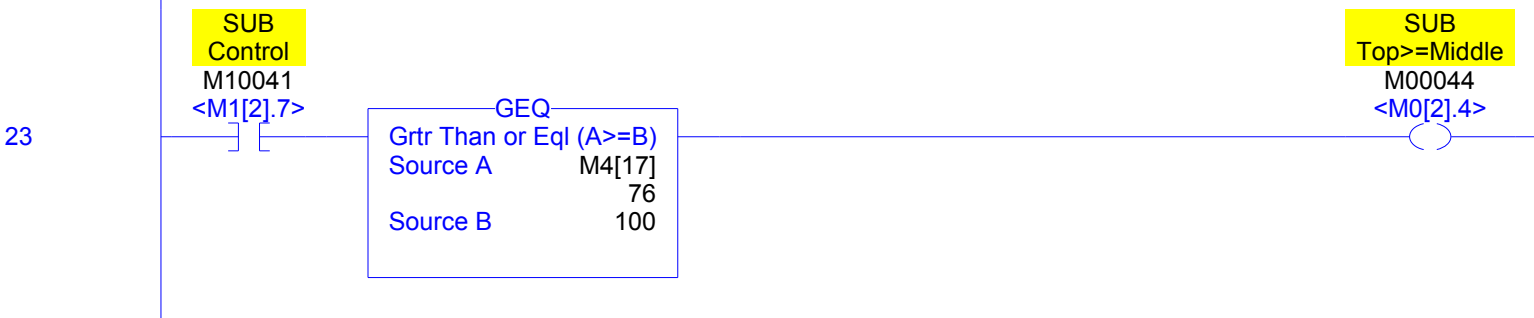
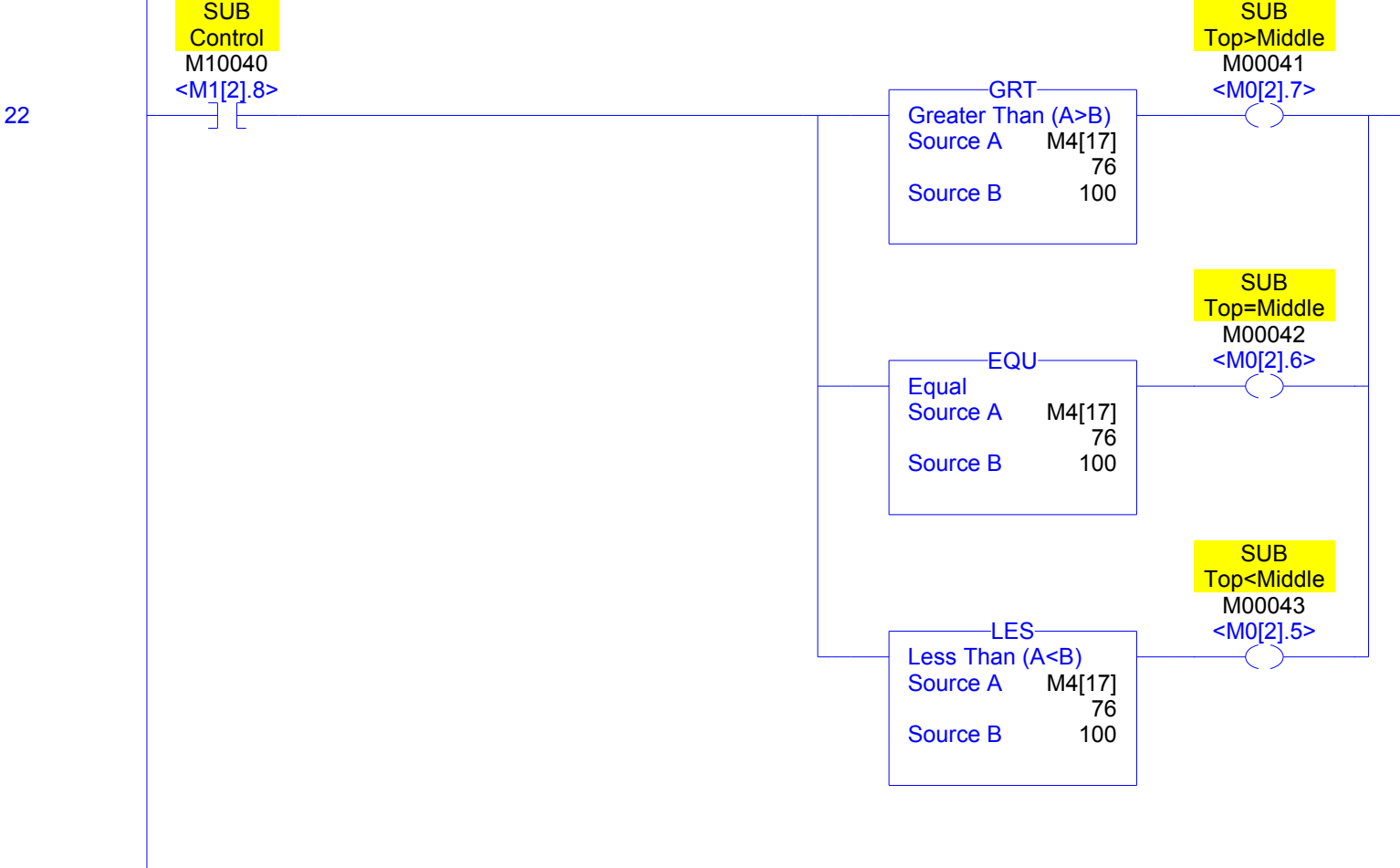




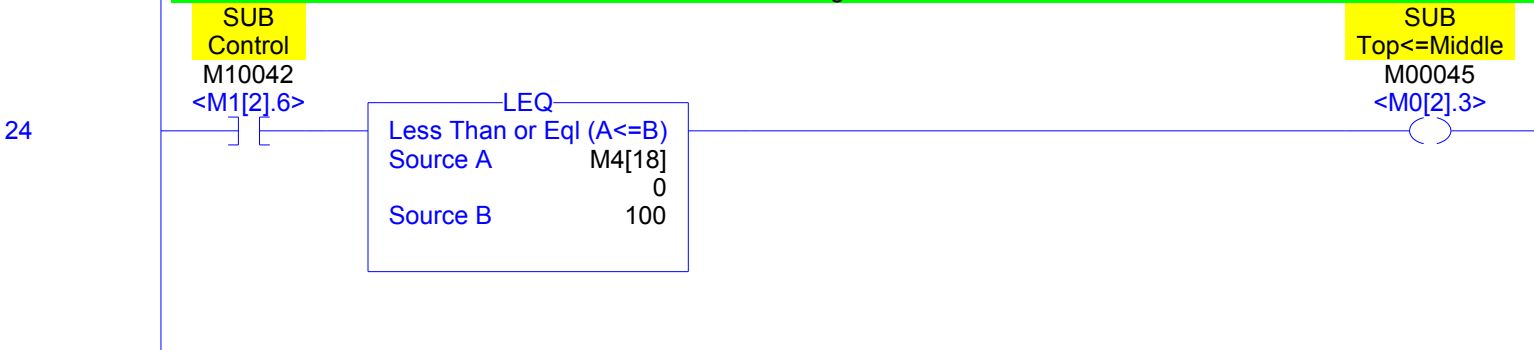




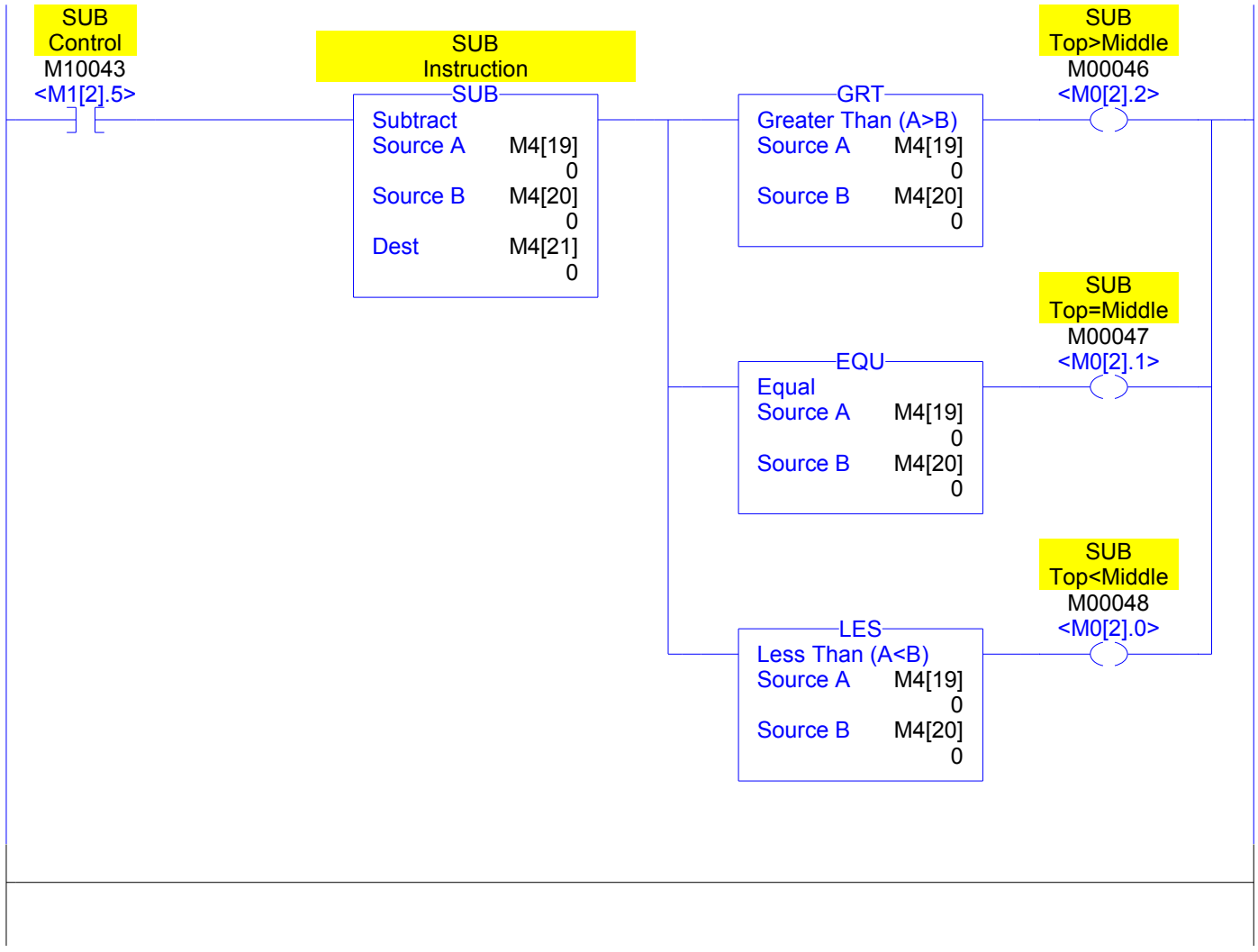
Network 8
Comparison
 When the SUB result contains the optional "Trash Resgister" the SUB instruction is removed and only the comparison is left.



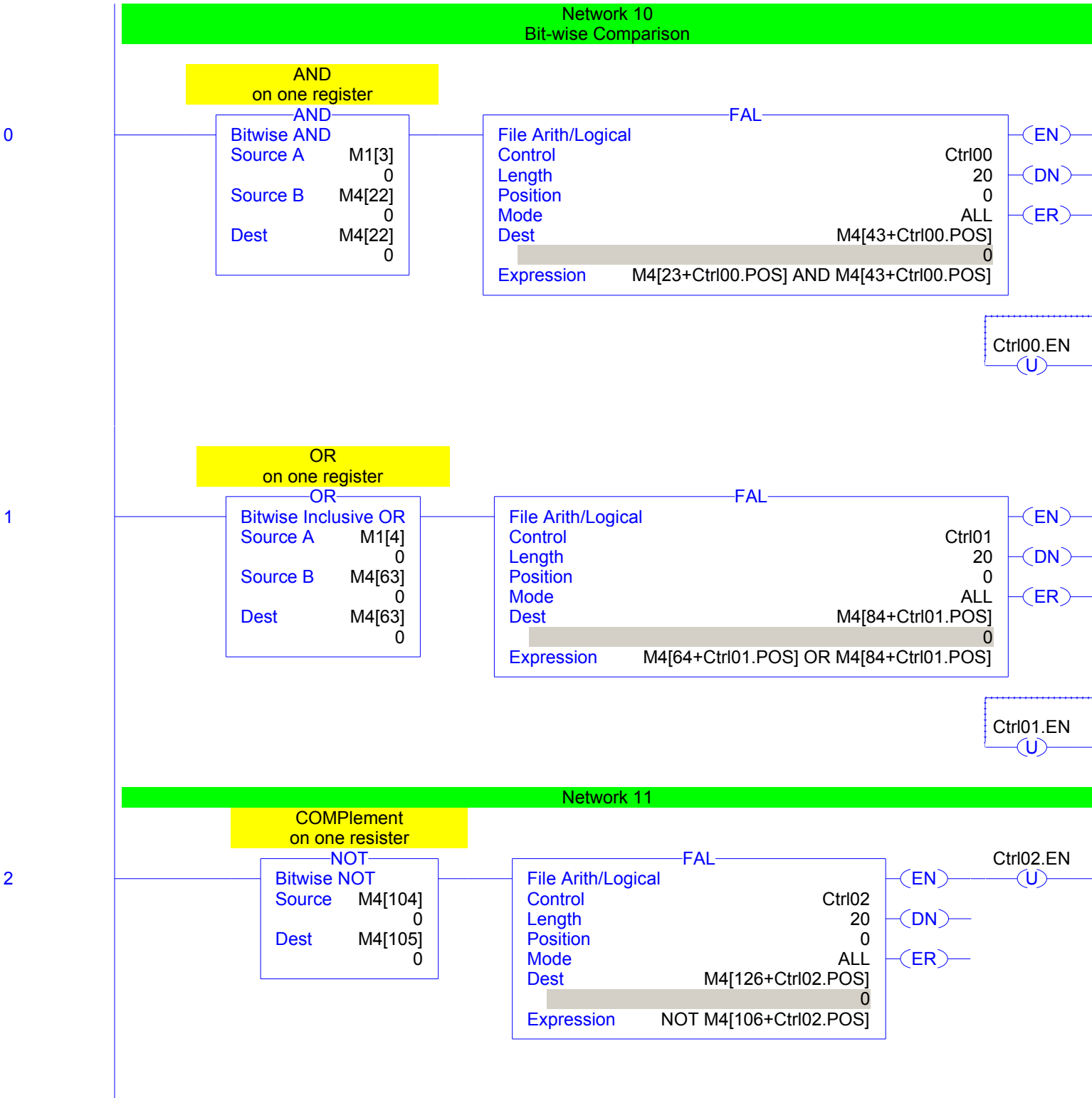
Network 9
 This will show what will happen to SUB instructions that do not contain the "Trash Register."



25



(End)



3

XOR on one register

XOR	
Bitwise Exclusive OR	
Source A	M4[146]
	0
Source B	M4[147]
	0
Dest	M4[147]
	0

File Arith/Logical	
Control	FAL
Length	20
Position	0
Mode	ALL
Dest	M4[168+Ctrl03.POS]
	0
Expression	M4[148+Ctrl03.POS] OR M4[168+Ctrl03.POS]

Ctrl03.EN
U

Network 12
Register and Table moves

4

SKP Control

M10026
<M1[1].6>

N14
JMP

e
e
e
e
e
e

R->T
Prevent
Pointer
Increment

M10028
<M1[1].4>

6

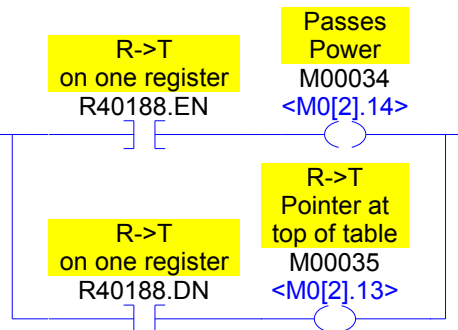
R->T
Control

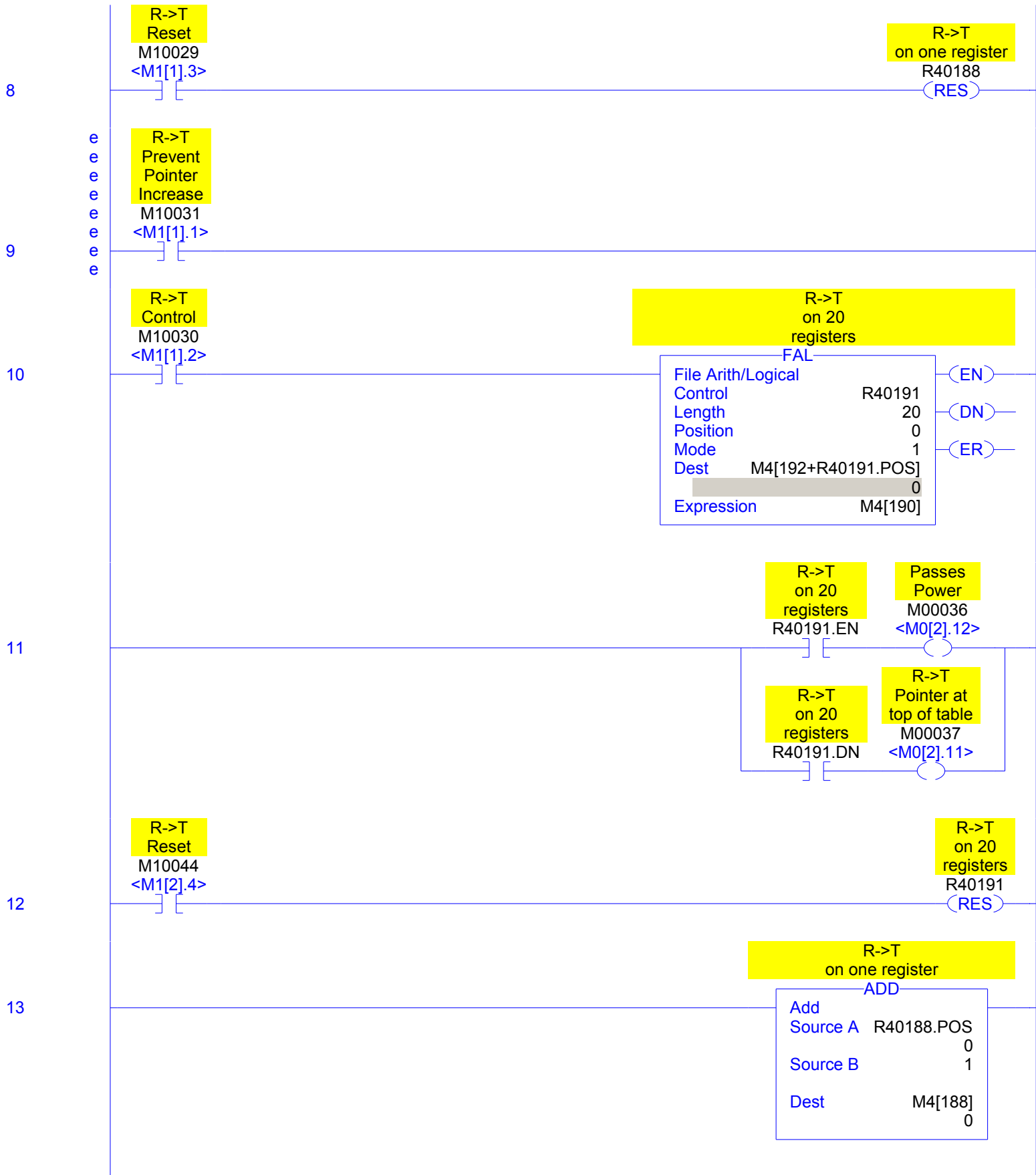
M10027
<M1[1].5>

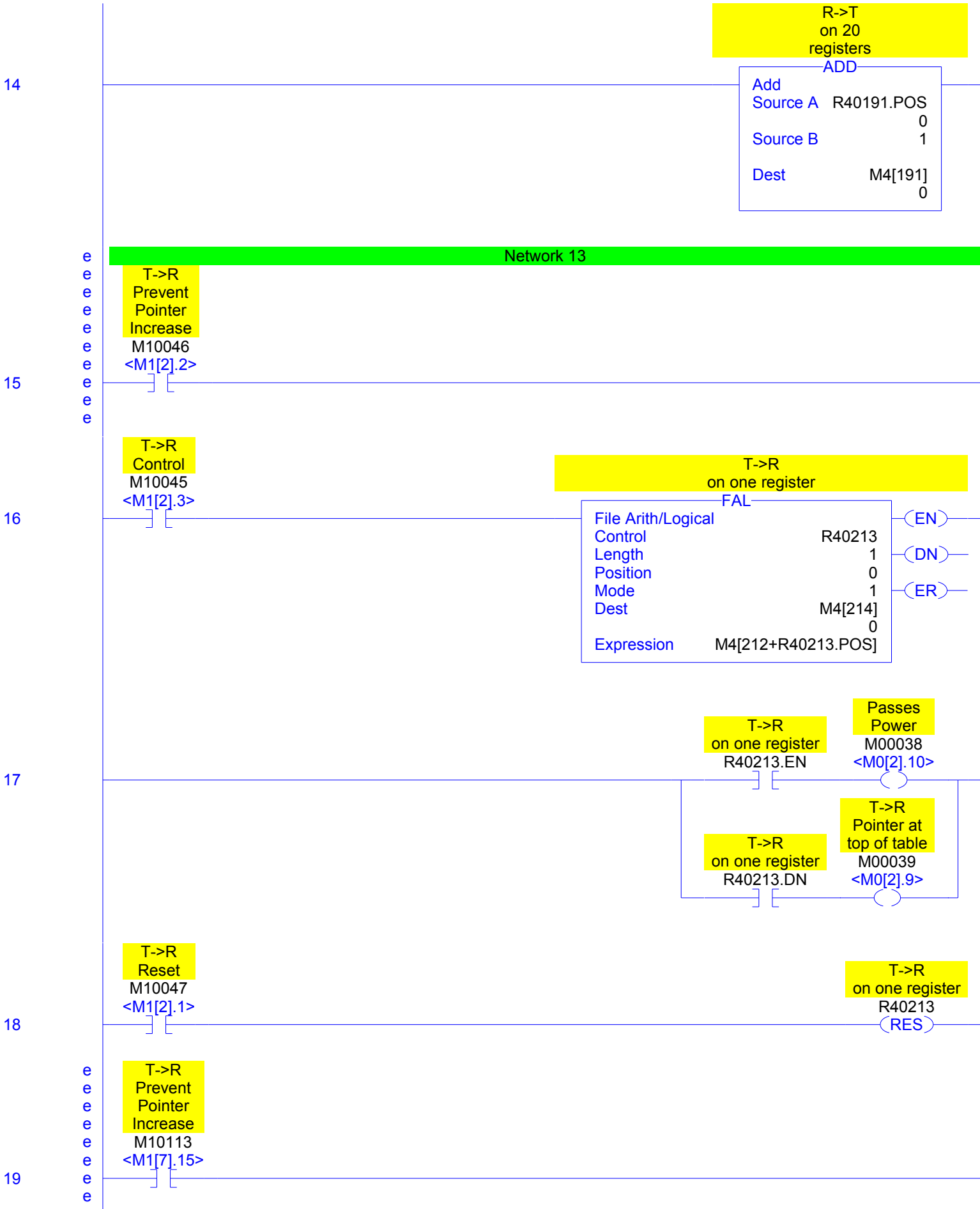
R->T on one register

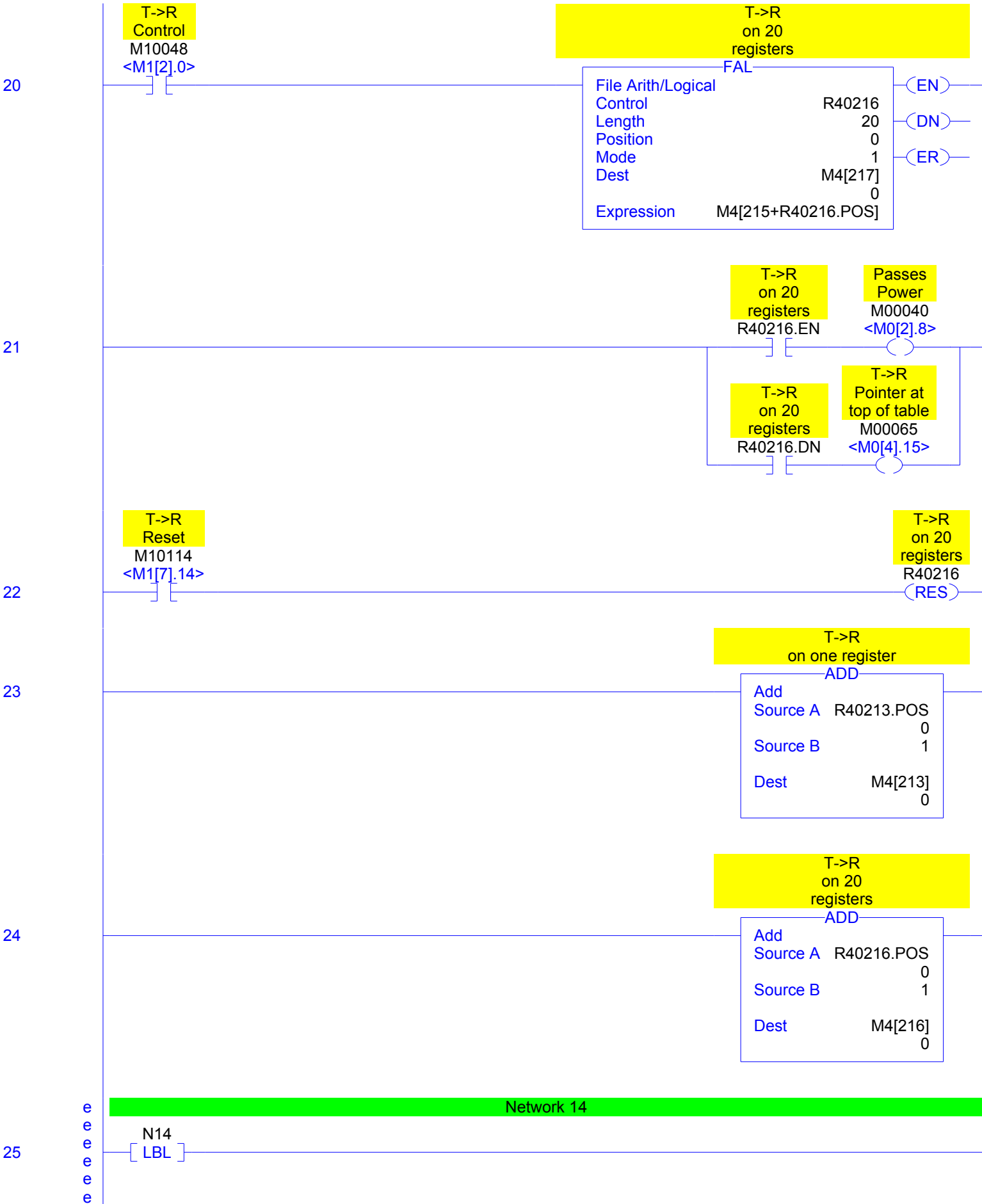
File Arith/Logical	
Control	R40188
Length	1
Position	0
Mode	1
Dest	M4[189+R40188.POS]
	0
Expression	M1[5]

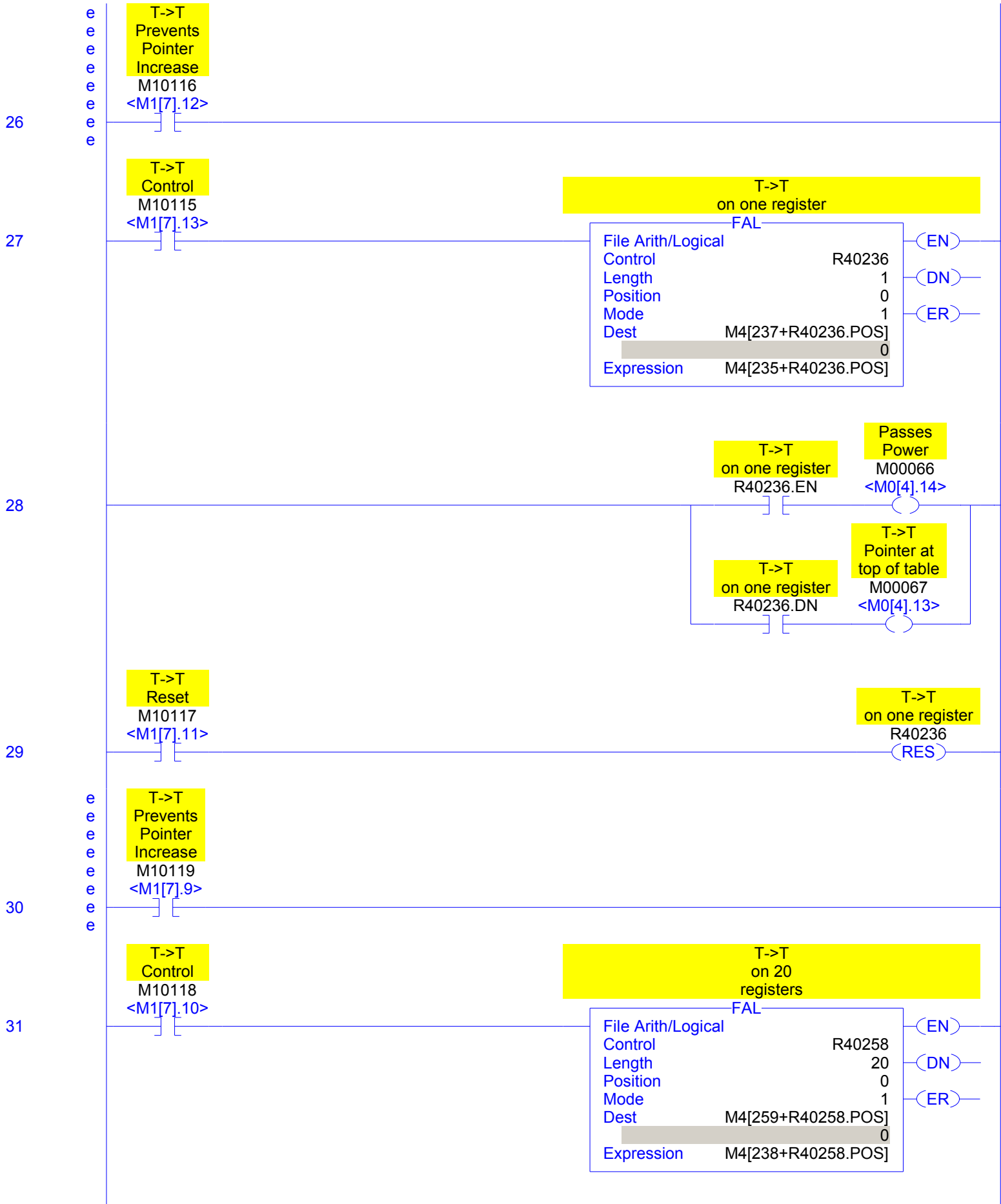
7

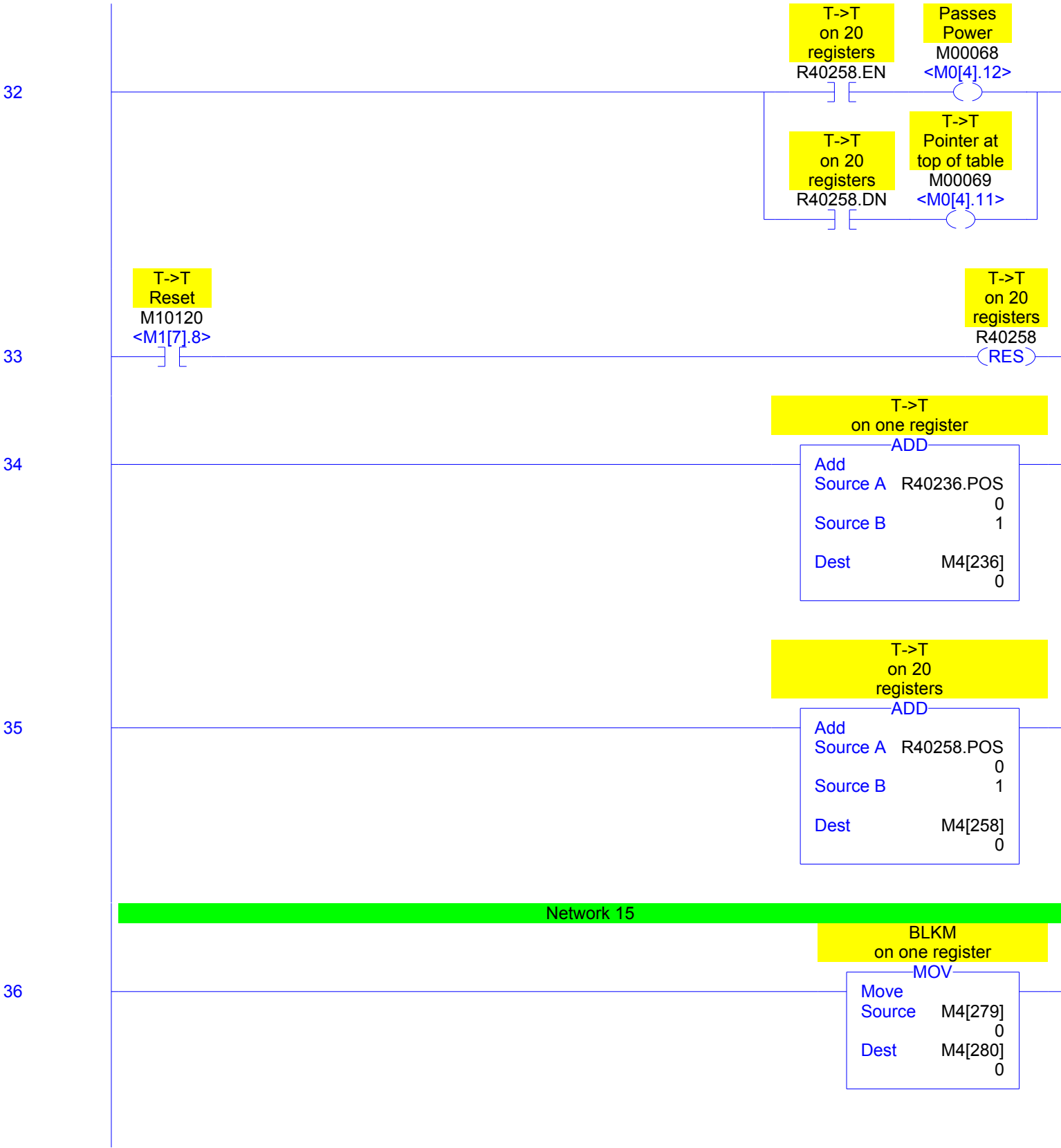










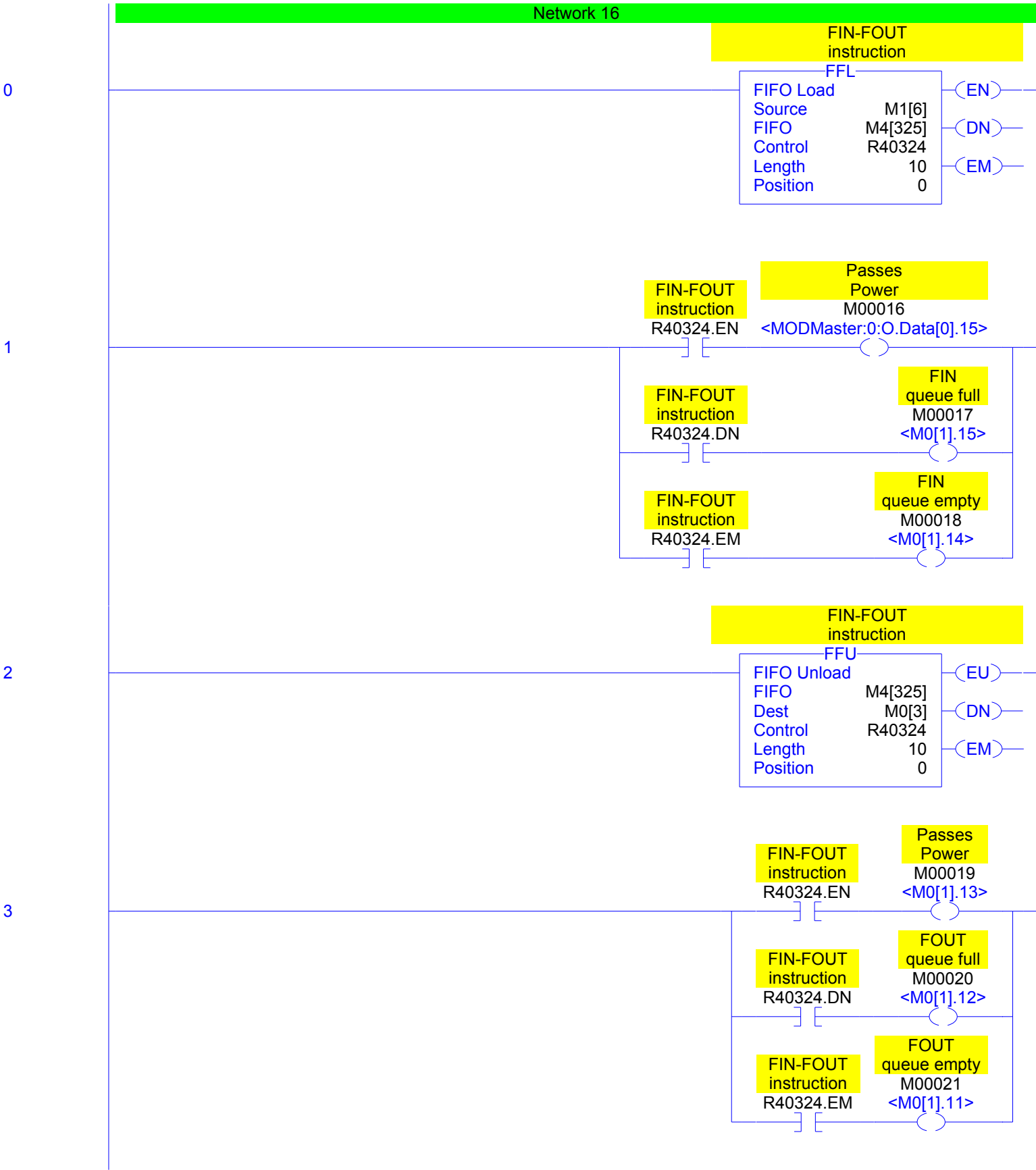


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BLKM
on 20
registers

COP
Copy File
Source M4[281]
Dest M4[301]
Length 20

(End)



4

FIN-FOUT instruction

ADD

Add	
Source A	R40324.POS
	0
Source B	1
Dest	M4[324]
	0

5

FIN-FOUT instruction

ADD

Add	
Source A	R40324.POS
	0
Source B	1
Dest	M4[324]
	0

e
e
e
e
e
e
e

Network 17

6

SRCH
Start search
at pointer
register
M10122
<M1[7].6>

7

SRCH
Control
M10121
<M1[7].7>

SRCH instruction

FSC

File Search/Compare		(EN)
Control	R40335	(DN)
Length	10	(ER)
Position	0	
Mode	ALL	
Expression	M4[321]=M4[336+R40335.POS]	

8

SRCH instruction	R40335.EN	Passes Power	M00077	<M0[4].3>
SRCH match found	M00031			<M0[1].1>
SRCH instruction	R40335.FD			

9
e
e
e
e
e
e
e
e

GSV
Get System Value

Class Name	?
Instance Name	?
Attribute Name	?
Dest	??

SRCH
instruction

10

ADD

Add	
Source A	R40335.POS
	0
Source B	1
Dest	M4[335]
	0

e
e
e
e
e
e
e
e

Network 18

11

CMPR
Reset
Pointer
M10124
<M1[7].4>

12

CMPR
Control
M10123
<M1[7].5>

CMPR
instruction
R40339.IN
(L)

COP

Copy File	
Source	M4[337]
Dest	DINTSource[0]
Length	1

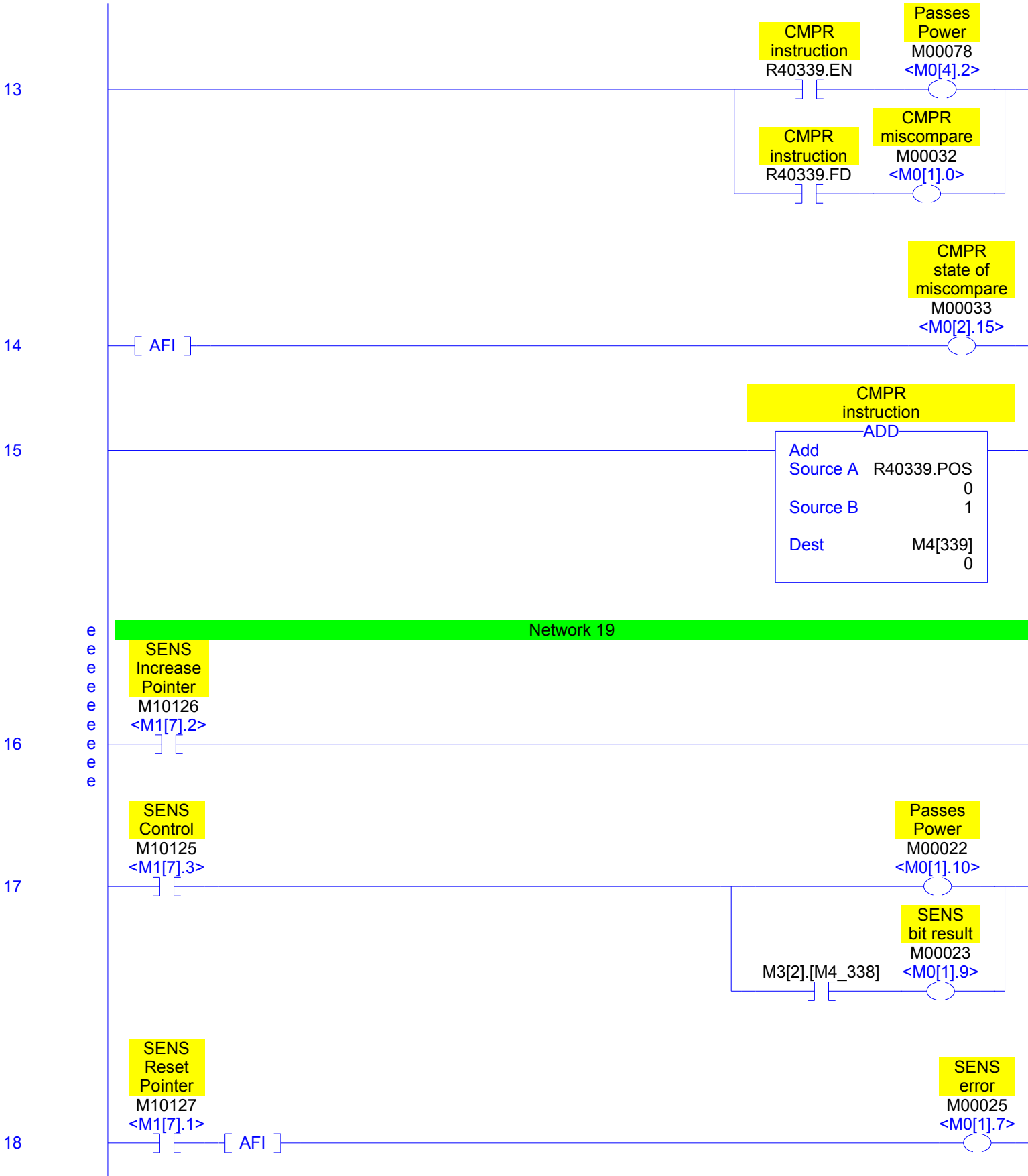
COP

Copy File	
Source	M4[340]
Dest	DINTReference[0]
Length	1

CMPR
instruction

FBC
File Bit Comparison

Source	DINTSource[0]	(EN)
Reference	DINTReference[0]	(DN)
Result	DINTResult[0]	
Cmp. Control	R40339	(FD)
Length	16	
Position	0	(IN)
Result Control	R40339_R	
Length	1	(ER)
Position	0	



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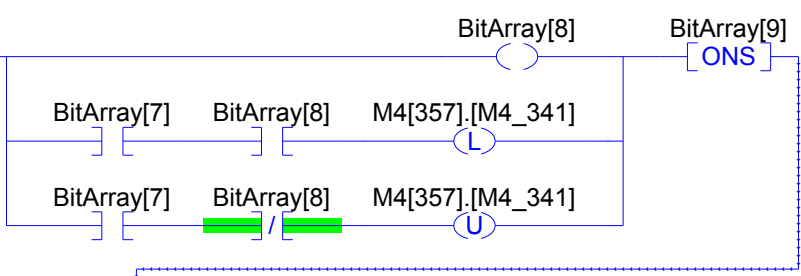
MBIT Control
M10128
<M1[7].0>

Passes Power
M00026
<M0[1].6>

BitArray[7]

20

MBIT Set/Clear Control
M10129
<M1[8].15>



MBIT instruction

LEQ
Less Than or Eq (A<=B)
Source A M4_341
 <M4[341]>
Source B 0
 260

MBIT instruction

ADD
Add
Source A M4_341
 <M4[341]>
Source B 0
 1
Dest M4_341
 <M4[341]>
 0

MBIT sense bit
M00027
<M0[1].5>

MBIT instruction

GRT
Greater Than (A>B)
Source A M4_341
 <M4[341]>
Source B 0
 260

MBIT instruction

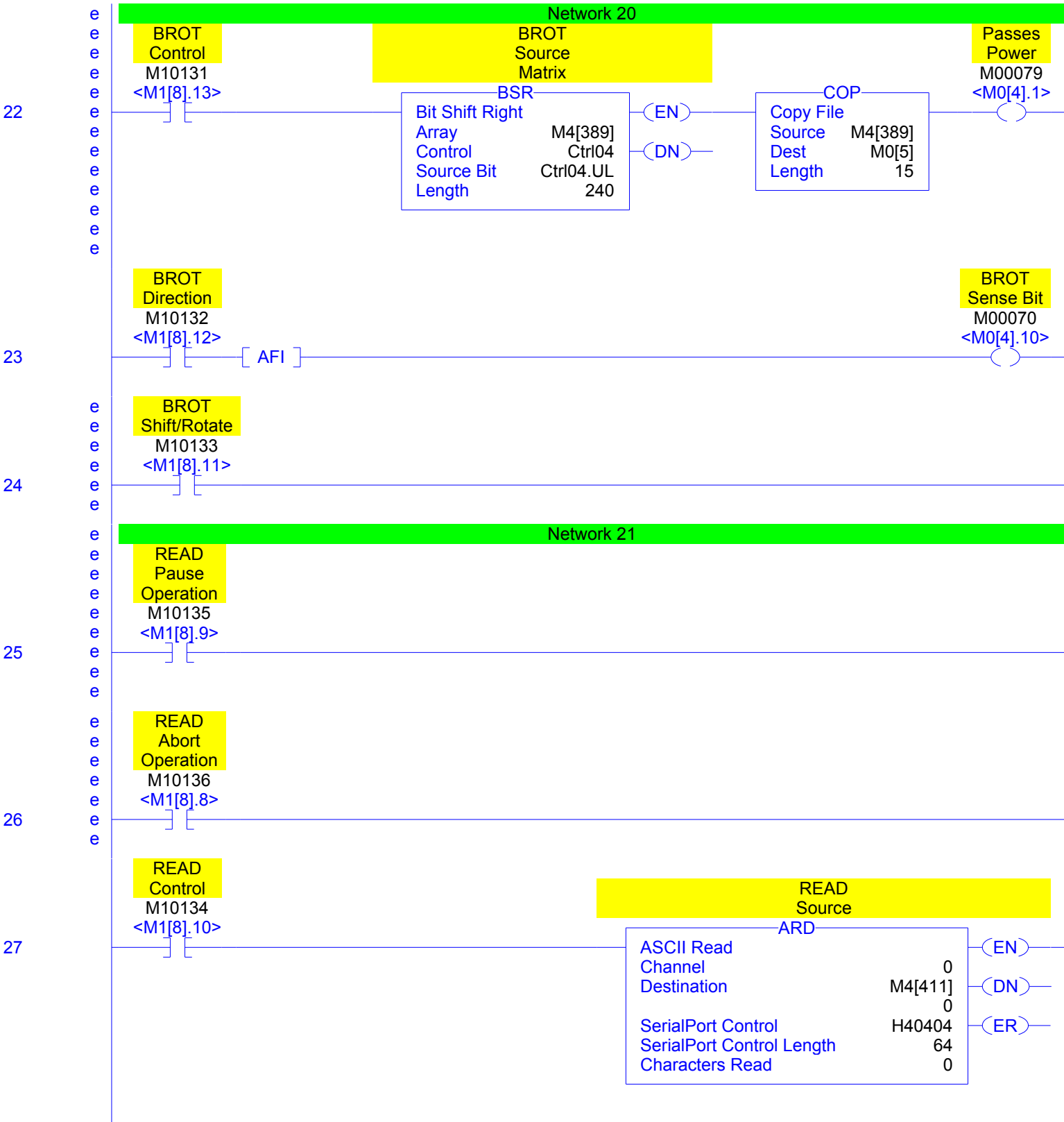
MOV
Move
Source 0
Dest M4_341
 <M4[341]>
 0

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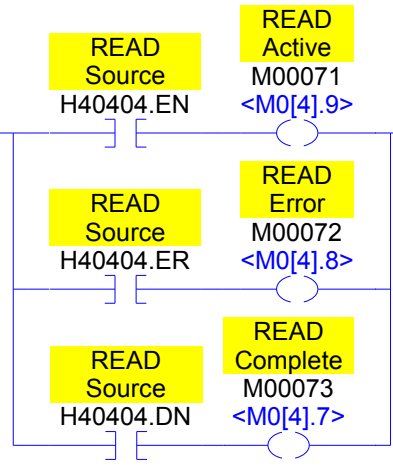
MBIT Increase Pointer
M10130
<M1[8].14>

[AFI]

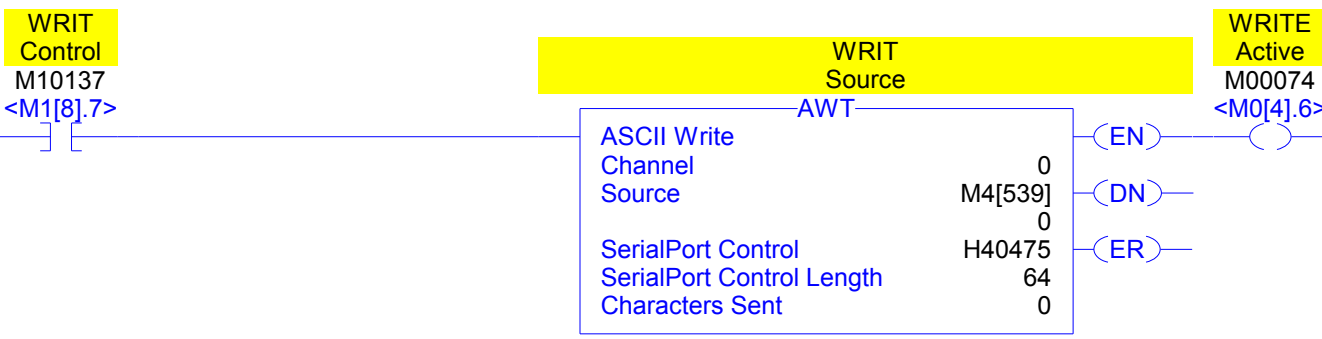
MBIT error
M00028
<M0[1].4>



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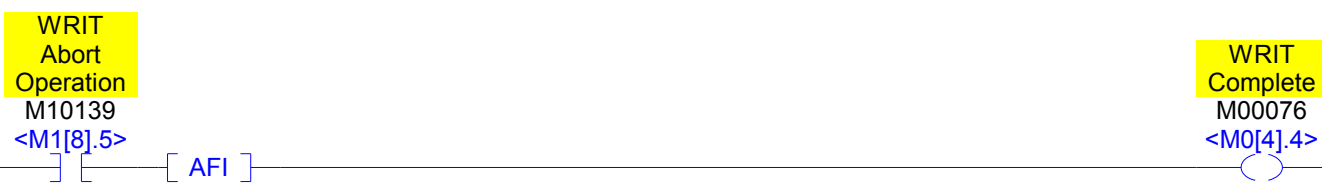
29



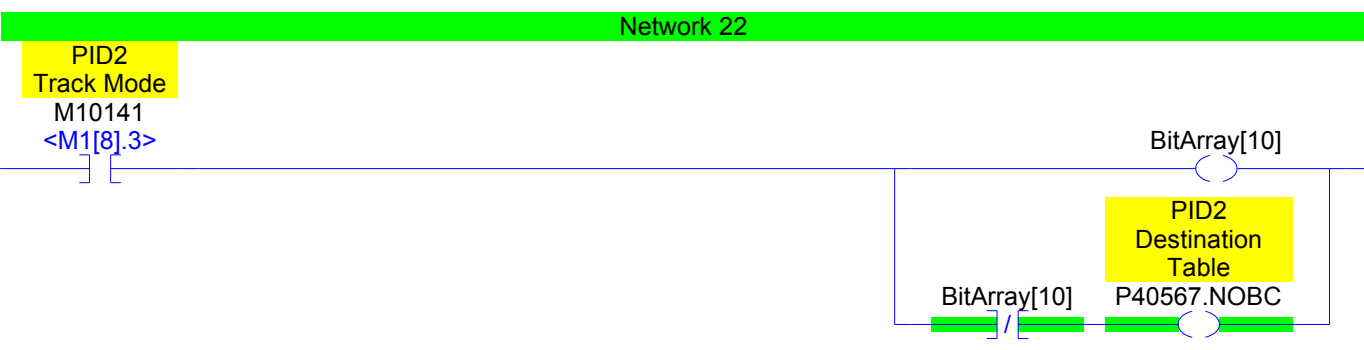
30



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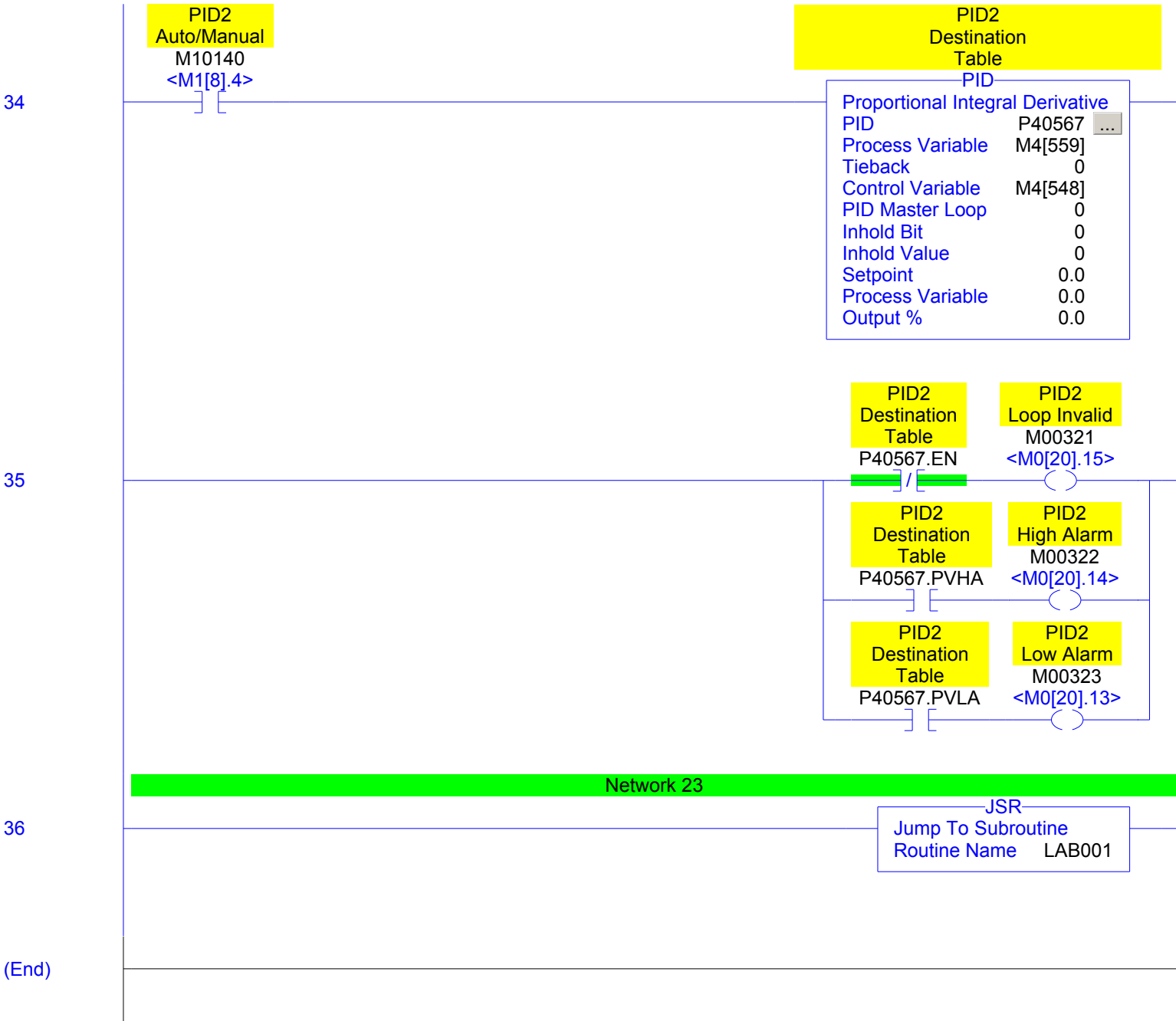


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(End)

